ISO^2-CMOS **MT91L62**

3 Volt Single Rail Codec

Advance Information

ISSUE 2 October 1996

Features

- Single 2.7-3.6 volt supply
- Programmable μ–law/A-law Codec and filters
- Fully differential to output driver
- SSI digital interface
- Individual transmit and receive mute controls
- 0dB gain in receive path
- 6dB gain in transmit path
- Low power operation
- ITU-T G.714 compliant

Applications

- Cellular radio sets
- Local area communications stations
- Line cards
- Battery operated equipment

Ordering Information

MT91L62AE	20 Pin Plastic DIP
MT91L62AS	20 Pin SOIC

-40°C to +85°C

Description

The MT91L62 3V single rail Codec incorporates a built-in Filter/Codec, transmit anti-alias filter, a reference voltage and bias source. The device supports both A-law and μ-law requirements. The MT91L62 is a true 3V device employing a fully differential architecture to ensure wide dynamic range.

An analog output driver is provided, capable of driving a 20k ohm load.

The MT91L62 is fabricated in Mitel's ISO^2-CMOS technology ensuring low power consumption and high reliability.

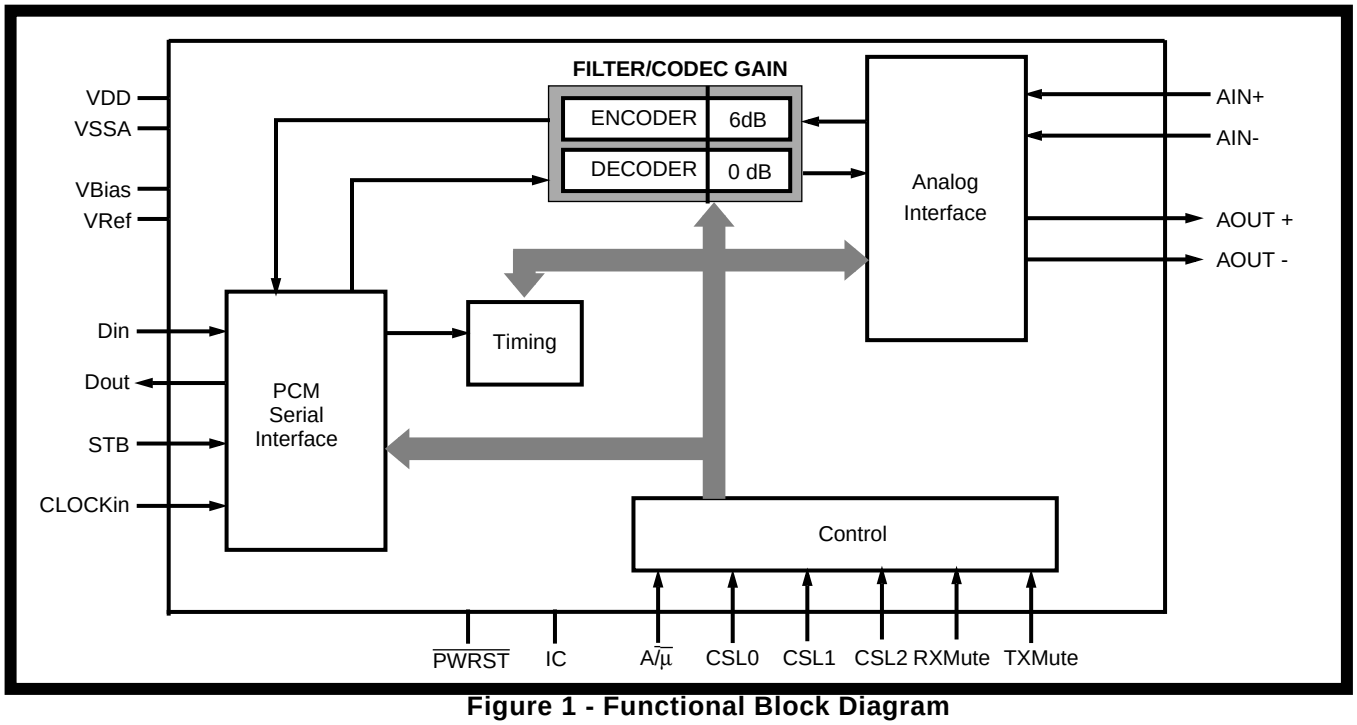
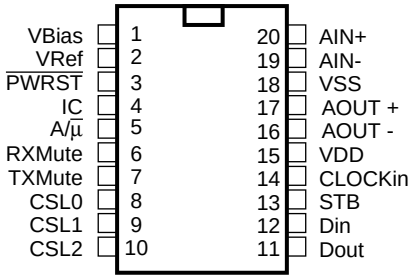


Figure 1 - Functional Block Diagram



20 PIN SOIC/PDIP

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
13	V_{Bias}	**Bias Voltage (Output).** (V_{DD}/2) volts is available at this pin for biasing external amplifiers. Connect 0.1 μ F capacitor to V_{SS}.
14	V_{Ref}	**Reference Voltage for Codec (Output).** Nominally [(V_{DD}/2)-1.1] volts. Used internally. Connect 0.1 μ F capacitor to V_{SS}.
15	$\overline{PWRST}$	**Power-up Reset.** Resets internal state of device via Schmitt Trigger input (active low).
16	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
17	A/$\overline{\mu}$	**A/$\overline{\mu}$ Law Selection**. CMOS level compatable input pin governs the companding law used by the device. A-law selected when pin tied to V_{DD} or μ-law selected when pin tied to V_{SS}.
18	RXMute	**Receive Mute.** When 1, the transmit PCM is forced to negative zero code. When 0, normal operation. CMOS level compatable input.
19	TXMute	**Transmit Mute.** When 1, the transmit PCM is forced to negative zero code. When 0, normal operation. CMOS level compatable input.
20 21 22	CSL0 CSL1 CSL2	**Clock Speed Select.** These pins are used to program the speed of the SSI mode as well as the conversion rate between the externally supplied MCL clock and the 512 KHz clock required by a filter/codec. Refer to Table 2 for details. CMOS level compatable input.
23	D_{out}	**Data Output.** A tri-state digital output for 8-bit wide channel data being sent to the Layer 1 device. Data is shifted out via the pin concurrent with the rising edge of BCL during the timeslot defined by STB.
24	D_{in}	**Data Input.** A digital input for 8-bit wide data from the layer 1 device. Data is sampled on the falling edge of BCL during the timeslot defined by STB. CMOS level compatable input.
13	STB	**Data Strobe.** This input determines the 8-bit timeslot used by the device for both transmit and receive data. This active high signal has a repetition rate of 8 kHz. CMOS level compatable input.
14	CLOCKin	**Clock (Input).** The clock provided to this input pin is used by the internal device functions. Connect bit clock to this pin when it is 512 kHz or greater. Connect a 4096 kHz clock to this pin when the bit clock is 128 kHz or 256 kHz. CMOS level compatable input.
15	V_{DD}	**Positive Power Supply.** Nominally 3 volts.
16	AOUT-	**Inverting Analog Output.** (balanced).
17	AOUT+	**Non-Inverting Analog Output.** (balanced).
18	V_{SS}	**Ground.** Nominally 0 volts.
19	Ain-	**Inverting Analog Input.** No external anti-aliasing is required.
20	Ain+	**Non-Inverting Analog Input.** Non-inverting input. No external anti-aliasing is required.

Overview

The 3V Single-Rail Codec features complete Analog/ Digital and Digital/Analog conversion of audio signals (Filter/Codec) and an analog interface to a standard analog transmitter and receiver (analog Interface). The receiver amplifier is capable of driving a 20k ohm load.

Functional Description

Filter/Codec

The Filter/Codec block implements conversion of the analog 0-3.3 kHz speech signals to/from the digital domain compatible with 64 kb/s PCM B-Channels. Selection of companding curves and digital code assignment are programmable. These are ITU-T G.711 A-law or μ-Law, with true-sign/Alternate Digit Inversion.

The Filter/Codec block also implements a transmit audio path gain in the analog domain. Figure 3 depicts the nominal half-channel for the MT91L62.

The internal architecture is fully differential to provide the best possible noise rejection as well as to allow a wide dynamic range from a single 3 volt supply design. This fully differential architecture is continued into the Analog Interface section to provide full chip realization of these capabilities for the external functions.

A reference voltage (V_{Ref}), for the conversion requirements of the Codec section, and a bias voltage (V_{Bias}), for biasing the internal analog sections, are both generated on-chip. V_{Bias} is also brought to an external pin so that it may be used for biasing external gain setting amplifiers. A 0.1μF capacitor must be connected from V_{Bias} to analog ground at all times. Likewise, although V_{Ref} may only be used internally, a 0.1μF capacitor from the V_{Ref} pin to ground is required at all times. The analog ground reference point for these two capacitors must be physically the same point. To facilitate this the V_{Ref} and V_{Bias} pins are situated on adjacent pins.

The transmit filter is designed to meet ITU-T G.714 specifications. An anti-aliasing filter is included. This is a second order lowpass implementation with a corner frequency at 25 kHz.

The receive filter is designed to meet ITU-T G.714 specifications. Filter response is peaked to compensate for the sinx/x attenuation caused by the 8 kHz sampling rate.

Companding law selection for the Filter/Codec is provided by the A/$\overline{\mu}$ companding control pin. Table 1 illustrates these choices.

Code	ITU-T (G.711)	
	μ-Law	A-Law
+ Full Scale	1000 0000	1010 1010
+ Zero	1111 1111	1101 0101
-Zero (quiet code)	0111 1111	0101 0101
- Full Scale	0000 0000	0010 1010

Table 1: Law Selection

Analog Interfaces

Standard interfaces are provided by the MT91L62. These are:

- The analog inputs (transmitter), pins AIN+/AIN-. The maximum peak to peak input is 2.123Vpp μ–law across AIN+/AIN- and 2.2Vpp A-law across these pins.
- The analog outputs (receiver), pins AOUT+/ AOUT-. This internally compensated fully differential output driver is capable of driving a load of 20k ohms.

PCM Serial Interface

A serial link is required to transport data between the MT91L62 and an external digital transmission device. The MT91L62 utilizes the strobed data interface found on many standard Codec devices. This interface is commonly referred to as Simple Serial Interface (SSI).

The bit clock rate is selected by setting the CSL2-0 control pins as shown in Figure 2.

Quiet Code

The PCM serial port can be made to send quiet code to the decoder and receive filter path by setting the RxMute pin high. Likewise, the PCM serial port will send quiet code in the transmit path when the

CSL_2	CSL_1	CSL_0	External Clock Bit Rate (kHz)	CLOCKin (kHz)
1	0	0	128	4096
1	0	1	256	4096
0	0	0	512	512
0	0	1	1536	1536
0	1	0	2048	2048
0	1	1	4096	4096

Table 2: Bit Clock Rate Selection

TxMute pin is high. When either of these pins are low their respective paths function normally. The -Zero entry of Table 1 is used for the quiet code definition.

SSI Mode

The SSI BUS consists of input and output serial data streams named Din and Dout respectively, a Clock input signal (CLOCKin), and a framing strobe input (STB). A 4.096 MHz master clock is also required for SSI operation if the bit clock is less than 512 kHz. The timing requirements for SSI are shown in Figures 5 & 6.

In SSI mode the MT91L62 supports only B-Channel operation. Hence, in SSI mode transmit and receive B-Channel data are always in the channel defined by the STB input.

The data strobe input STB determines the 8-bit timeslot used by the device for both transmit and receive data. This is an active high signal with an 8 kHz repetition rate.

SSI operation is separated into two categories based upon the data rate of the available bit clock. If the bit clock is 512 kHz or greater then it is used directly by the internal MT91L62 functions allowing synchronous operation. If the available bit clock is 128 kHz or 256 kHz, then a 4096 kHz master clock is required to derive clocks for the internal MT91L62 functions.

Applications where Bit Clock (BCL) is below 512 kHz are designated as asynchronous. The MT91L62 will re-align its internal clocks to allow operation when the external master and bit clocks are asynchronous. Control pins CSL2, CSL1 and CSL0 are used to program the bit rates.

For synchronous operation, data is sampled from Din, on the falling edge of BCL during the time slot defined by the STB input. Data is made available, on

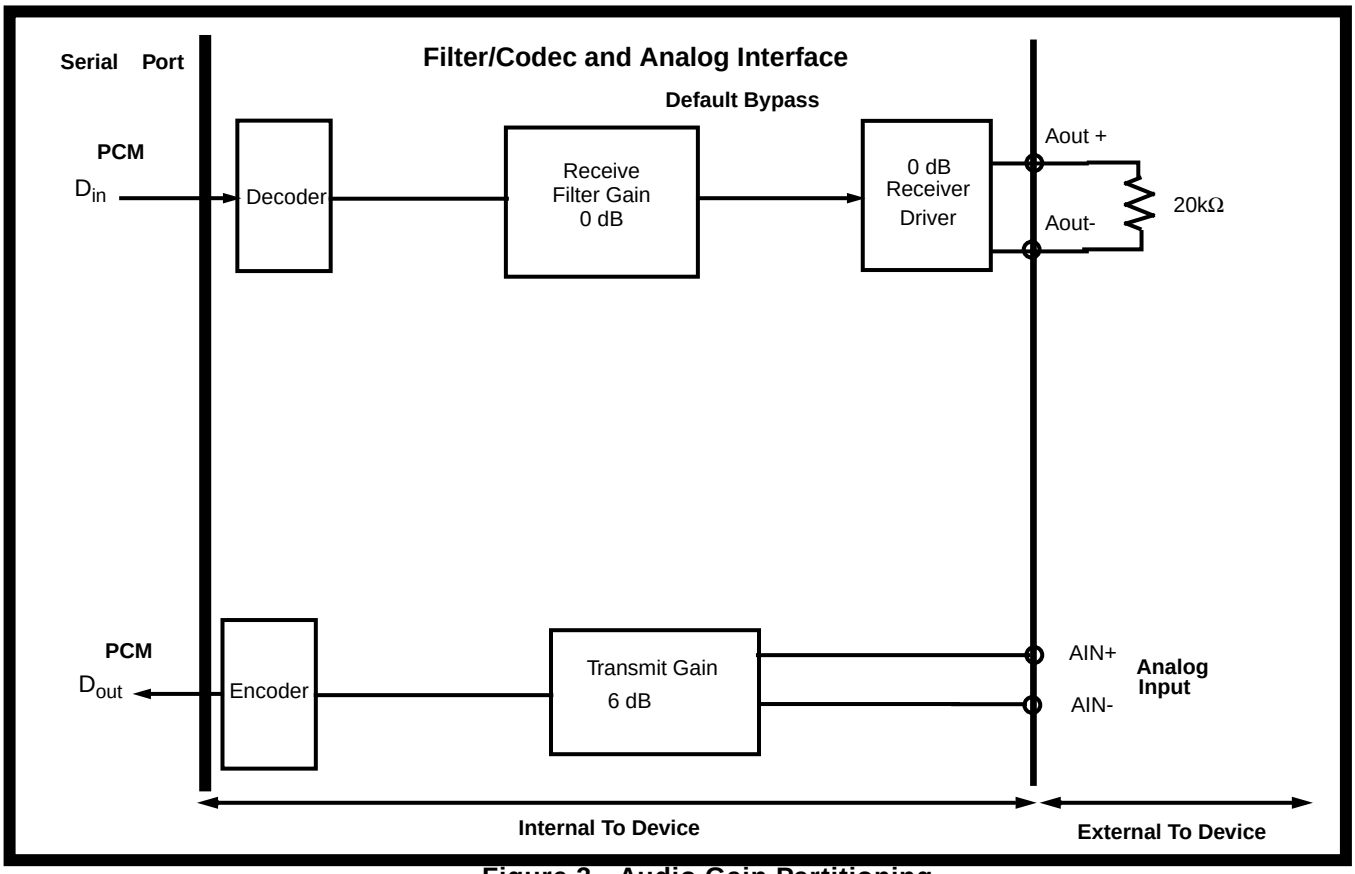


Figure 3 - Audio Gain Partitioning

Dout, on the rising edge of BCL during the time slot defined by the STB input. Dout is tri-stated at all times when STB is not true. If STB is valid, then quiet code will be transmitted on Dout during the valid strobe period. There is no frame delay through the PCM serial circuit for synchronous operation.

For asynchronous operation Dout and Din are as defined for synchronous operation except that the allowed output jitter on Dout is larger. This is due to the resynchronization circuitry activity and will not affect operation since the bit cell period at 128 kb/s and 256 kb/s is relatively large. There is a one frame delay through the PCM serial circuit for asynchronous operation. Refer to the specifications of Figures 5 & 6 for both synchronous and asynchronous SSI timing.

$\overline{\text{PWRST}}$

While the MT91L62 is held in $\overline{\text{PWRST}}$ no device control or functionality is possible.

Applications

Figure 4 shows an application of the MT91L62 in a line card.

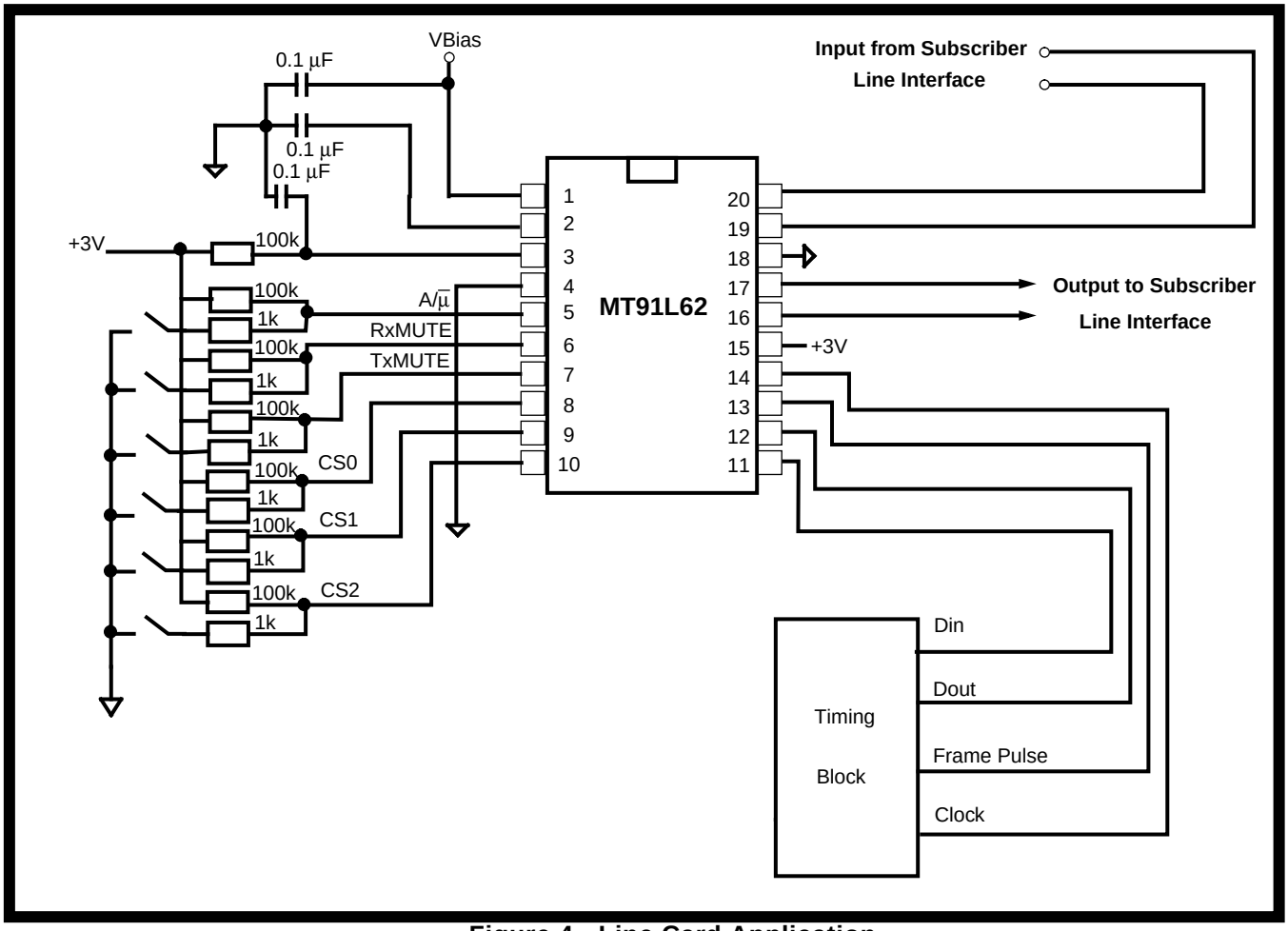


Figure 4 - Line Card Application

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD} - V_{SS}	- 0.3	5	V
2	Voltage on any I/O pin	V_I/V_O	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current on any I/O pin (transducers excluded)	I_I/I_O		± 20	mA
4	Storage Temperature	T_S	- 65	+ 150	°C
5	Power Dissipation (package)	P_D		750	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	2.7	3	3.6	V	
2	CMOS Input Voltage (high)	V_{IHC}	0.9*V_{DD}		V_{DD}	V	
3	CMOS Input Voltage (low)	V_{ILC}	V_{SS}		0.1*V_{DD}	V	
4	Operating Temperature	T_A	- 40		+ 85	°C	

Power Characteristics

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Static Supply Current (clock disabled)	I_{DDC1}		200		µA	Outputs unloaded, Input signals static, not loaded
2	Dynamic Supply Current: Total all functions enabled	I_{DDFT}		4.8		mA	See Note 1.

Note 1: Power delivered to the load is in addition to the bias current requirements.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input HIGH Voltage CMOS inputs	V_{IHC}	2.1			V	
2	Input LOW Voltage CMOS inputs	V_{ILC}			0.9	V	
3	VBias Voltage Output	V_{Bias}		$V_{DD}/2$		V	Max. Load = 10kΩ
4	V_{Ref} Output Voltage	V_{Ref}		$V_{DD}/2$-1.1		V	No load
5	Input Leakage Current	I_{IZ}		0.1	10	µA	$V_{IN}=V_{DD}$ to V_{SS}
6	Positive Going Threshold Voltage ($\overline{PWRST}$ only) Negative Going Threshold Voltage ($\overline{PWRST}$ only)	V_{T+} V_{T-}	2.2		 0.8	V V	
7	Output HIGH Current	I_{OH}		1.25		mA	$V_{OH} = 0.9*V_{DD}$ See Note 1
8	Output LOW Current	I_{OL}		2.5		mA	$V_{OL} = 0.1*V_{DD}$ See Note 1
9	Output Leakage Current	I_{OZ}		0.01	10	µA	$V_{OUT} = V_{DD}$ and V_{SS}
10	Output Capacitance	C_o		15		pF	
11	Input Capacitance	C_i		10		pF	

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

* Note 1 - Magnitude measurement, ignore signs.

Clockin Tolerance Characteristics†

	Characteristics	Min	Typ‡	Max	Units	Test Conditions
1	CLOCKin Frequency (Asynchronous Mode)	4095.6	4096	4096.4	kHz	(i.e. 100 ppm)

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Characteristics† for A/D (Transmit) Path - 0dBm0 = $A_{Lo3.17}$ - 3.17dB = 1.027V_{rms} for μ-Law and 0dBm0 = $A_{Lo3.14}$ - 3.14dB =1.067V_{rms} for A-Law, at the Codec. (V_{Ref}=0.4 volts and V_{Bias}=1.5 volts.)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Analog input equivalent to overload decision	$A_{Li3.17}$ $A_{Li3.14}$		4.246 4.4		Vp-p Vp-p	μ-Law A-Law Both at Codec
2	Absolute half-channel gain M ± to Dout	 G_{AX1}		 6.0		 dB	Transmit filter gain=0dB setting. @1020Hz
3	Gain tracking vs. input level ITU-T G.714 Method 2	G_{TX}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total Distortion vs. input level. ITU-T G.714 Method 2	D_{QX}	35 29 24			dB dB dB	0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Transmit Idle Channel Noise	N_{CX} N_{PX}		15 -70	16.5 -69	dBrnC0 dBm0p	μ-Law A-Law
6	Gain relative to gain at 1020Hz <50Hz 60Hz 200Hz 300 - 3000 Hz 3000 - 3400 Hz 4000 Hz >4600 Hz	G_{RX}	 -0.25 -0.9 		 -25 -30 0.0 0.25 0.25 -12.5 -25	 dB dB dB dB dB dB dB	
7	Absolute Delay	D_{AX}		360		μs	at frequency of minimum delay
8	Group Delay relative to D_{AX}	D_{DX}		750 380 130 750		μs μs μs μs	500-600 Hz 600 - 1000 Hz 1000 - 2600 Hz 2600 - 2800 Hz
9	Power Supply Rejection f=1020 Hz f=0.3 to 3 kHz f=3 to 4 kHz f=4 to 50 kHz	 PSSR PSSR1 PSSR2 PSSR3		 37 40 35 40		 dB dB dB dB	±100mV peak signal on V_{DD} μ-law PSSR1-3 not production tested

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Characteristics† for D/A (Receive) Path - 0dBm0 = $A_{Lo3.17}$ - 3.17dB = 1.027V_{rms} for μ-Law and 0dBm0 = $A_{Lo3.14}$ - 3.14dB =1.067V_{rms} for A-Law, at the Codec. (V_{Ref}=0.4 volts and V_{Bias}=1.5 volts.)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Analog output at the Codec full scale	$A_{Lo3.17}$ $A_{Lo3.14}$		4.183 4.331		Vp-p Vp-p	μ-Law A-Law
1	Analog output at the CODEC full scale.	$A_{Lo3.17}$ $A_{Lo3.14}$		4.183 4.331		V_{p-p} V_{p-p}	μ-Law A-Law
2	Absolute half-channel gain. Din to HSPKR±	G_{AR1}		0		dB	@1020Hz
3	Gain tracking vs. input level ITU-T G.714 Method 2	G_{TR}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total distortion vs. input level. ITU-T G.714 Method 2	G_{QR}	35 29 24			dB dB dB	0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Receive Idle Channel Noise	N_{CR} N_{PR}		13 -77	15.5 -75	dBrnC0 dBm0p	μ-Law A-Law
6	Gain relative to gain at 1020Hz 200Hz 300 - 3000 Hz 3000 - 3400 Hz 4000 Hz >4600 Hz	G_{RR}	 -0.25 -0.90		 0.25 0.25 0.25 -12.5 -25	 dB dB dB dB dB	
7	Absolute Delay	D_{AR}		240		μs	at frequency of min. delay
8	Group Delay relative to D_{AR}	D_{DR}		750 380 130 750		μs μs μs μs	500-600 Hz 600 - 1000 Hz 1000 - 2600 Hz 2600 - 2800 Hz
9	Crosstalk D/A to A/D A/D to D/A	CT_{RT} CT_{TR}			-74 -80	dB dB	G.714.16 ITU-T

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics† for Analog Outputs

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Output load impedance	E_{ZL}	20k			ohms	across AOUT±
2	Allowable output capacitive load	E_{CL}		20		pF	each pin: AOUT+, AOUT-
3	Analog output harmonic distortion	E_D			0.5	%	20k ohms load across AOUT± (tol-15%), VO≤500mV_{RMS},,Rx gain=0dB

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‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics† for Analog Inputs

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input voltage overload level across AOUT+/AOUT-	V_{IOLH}		2.123 2.2		Vp-p Vp-p	$A/\overline{\mu} = 0$ $A/\mu = 1$
2	Input Impedance	Z_I	50			kΩ	Ain+/Ain- to V_{SS}

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - SSI BUS Synchronous Timing (see Figure 5)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	BCL Clock Period	t_{BCL}	244		1953	ns	BCL=4096 kHz to 512 kHz
2	BCL Pulse Width High	t_{BCLH}		122		ns	BCL=4096 kHz
3	BCL Pulse Width Low	t_{BCLL}		122		ns	BCL=4096 kHz
4	BCL Rise/Fall Time	t_R/t_F		20		ns	Note 1
5	Strobe Pulse Width	t_{ENW}		8 x t_{BCL}		ns	Note 1
6	Strobe setup time before BCL falling	t_{SSS}	80		t_{BCL}-80	ns	
7	Strobe hold time after BCL falling	t_{SSH}	80		t_{BCL}-80	ns	
8	Dout High Impedance to Active Low from Strobe rising	t_{DOZL}			90	ns	C_L=150 pF, R_L=1K
9	Dout High Impedance to Active High from Strobe rising	t_{DOZH}			90	ns	C_L=150 pF, R_L=1K
10	Dout Active Low to High Impedance from Strobe falling	t_{DOLZ}			90	ns	C_L=150 pF, R_L=1K
11	Dout Active High to High Impedance from Strobe falling	t_{DOHZ}			90	ns	C_L=150 pF, R_L=1K
12	Dout Delay (high and low) from BCL rising	t_{DD}			90	ns	C_L=150 pF, R_L=1K
13	Din Setup time before BCL falling	t_{DIS}	50			ns	
14	Din Hold Time from BCL falling	t_{DIH}	50			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
NOTE 1: Not production tested, guaranteed by design.

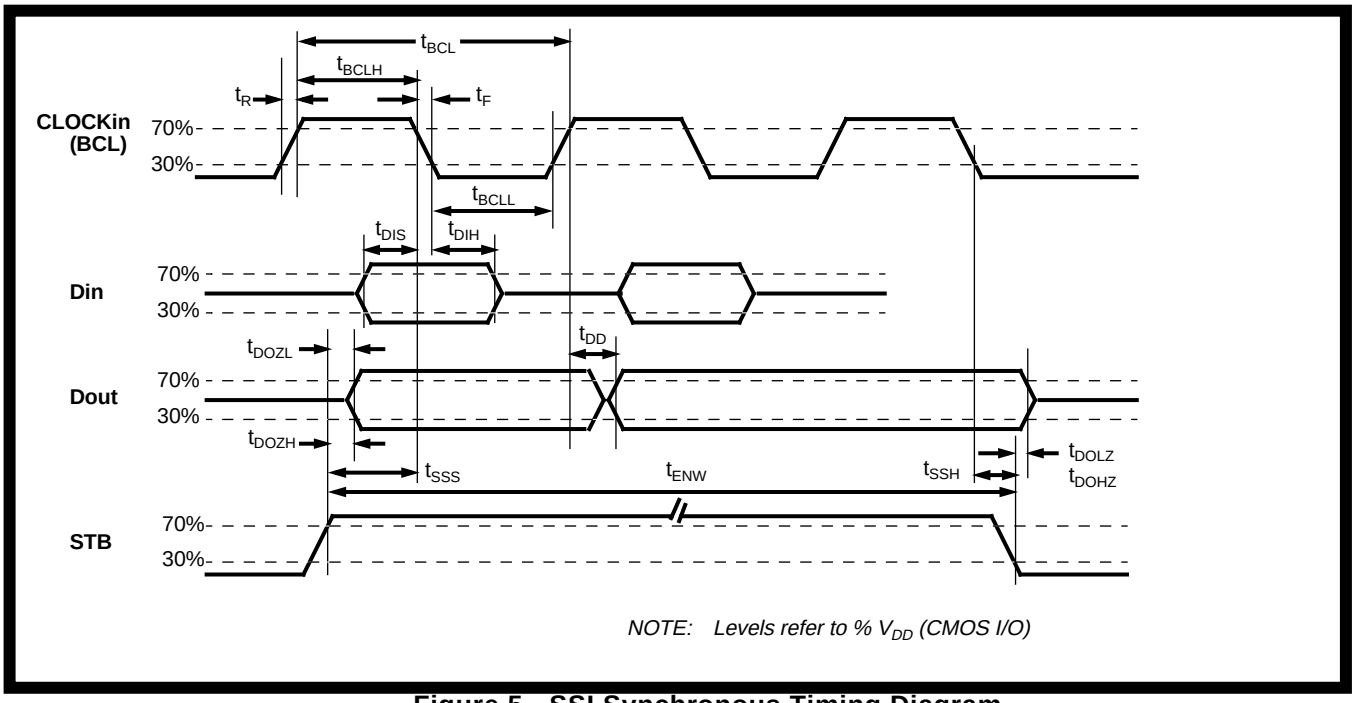

Figure 5 - SSI Synchronous Timing Diagram

AC Electrical Characteristics† - SSI BUS Asynchronous Timing (note 1) (see Figure 6)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Bit Cell Period	T_{DATA}		7812 3906		ns ns	BCL=128 kHz BCL=256 kHz
2	Frame Jitter	T_j			600	ns	
3	Bit 1 Dout Delay from STB going high	t_{dda1}			T_j+600	ns	C_L=150 pF, R_L=1K
4	Bit 2 Dout Delay from STB going high	t_{dda2}	600+ T_{DATA}-T_j	600+ T_{DATA}	600 + T_{DATA}+T_j	ns	C_L=150 pF, R_L=1K
5	Bit n Dout Delay from STB going high	t_{ddan}	600 + (n-1) x T_{DATA}-T_j	600 + (n-1) x T_{DATA}	600 + (n-1) x T_{DATA}+T_j	ns	C_L=150 pF, R_L=1K n=3 to 8
6	Bit 1 Data Boundary	T_{DATA1}	T_{DATA}-T_j		T_{DATA}+T_j	ns	
7	Din Bit n Data Setup time from STB rising	t_{SU}	T_{DATA}\2 +500ns-T_j +(n-1) x T_{DATA}			ns	n=1-8
8	Din Data Hold time from STB rising	t_{ho}	T_{DATA}\2 +500ns+T_j +(n-1) x T_{DATA}			ns	

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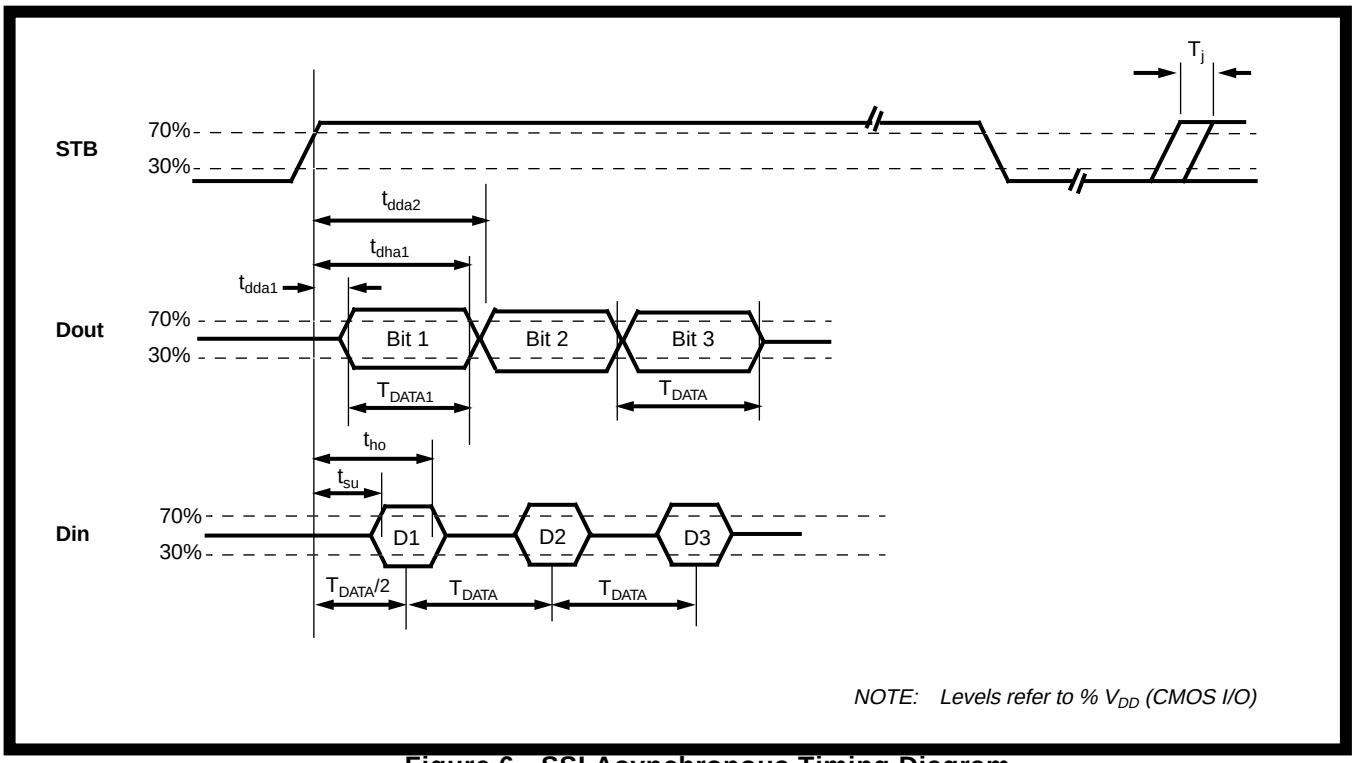

Figure 6 - SSI Asynchronous Timing Diagram